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A NEW PROPORTIONAL-INTEGRAL-DERIVATIVE (PID) CONTROLLER REALIZATION BY USING CURRENT CONVEYORS AND CALCULATING OPTIMUM PARAMETER TOLERANCES

AKIM TAÞIYICILAR KULLANARAK YENÝ BÝR ORANTI-ÝNTEGRAL-TÜREV (PÝD) TÝPÝ KONTROL EDÝCÝ GERÇEKLEME VE OPTÝMUM PARAMETRE TOLERANSLARININ HESAPLANMASI

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ABSTRACT

In process control industry, the proportional-integral-derivative (PID) controllers are one of the most important control elements. In practice, operational amplifiers are generally used in analog controllers. On the other hand, current-mode (CM) circuits such as second-generation current conveyors (CCII) and current feedback operational amplifiers (CFOA) have considerable attention due to their wider frequency band, lower power consumption, better linearity and stability properties compared to their voltage-mode counterparts, operational amplifiers. The purpose of this study is to present a synthesis procedure for the realization of analog PID controller by the use of CCIIs. For the designed PID circuit, the optimum parameter tolerances are determined. These tolerances can be used to improve and to control the sensitivity performance of the proposed PID controller.

Key words: *PID controller, current conveyor, and optimum parameter tolerances.*

ÖZET

Süreç kontrol endüstrisinde, orantý-türev-integral (PÝD) tip kontrolörler en önemli kontrol elemanlarýndan biridir. Uygulamada, analog kontrolörlerde genellikle iþlemsel kuvvetlendiriciler kullanýlmaktadýr. Öte yandan ikinci nesil akým taþýyýcý ve akým geri beslemeli iþlemsel kuvvetlendiriciler gibi akým çýkýþlý olarak çalýþan devreler, iþlemsel kuvvetlendiricilerle karþýlaþtýrýldýklarýnda daha geniþ bir frekans bandýna, daha düþük güç tüketimi ile çalýþma, ve daha iyi doðrusallýk ve kararlýlýk özelliklerine sahip olduklarýndan, son zamanlarda oldukça çok dikkat çekmektedirler. Bu çalýþmanýn amacý akým taþýyýcýlar (CCII) kullanarak bir analog kontrolör gerçeklemek için gerekli tasarým yöntemini vermektir. Tasarýmý yapýlan PID devresi için optimum parametre toleranslarý hesaplanmýþtýr. Bu toleranslar önerilen PID kontrol edicinin duyarlýk davranýþýnýn iyileþtirilmesi ve kontrol edilmesinde kullanýlabilirler.

Anahtar kelimeler: *PÝD kontrolör, akým taþýyýcý ve optimum parametre toleranslarý.*

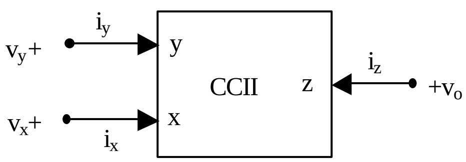
1. INTRODUCTION

The proportional-integral-derivative (PID) controllers are one of the most important control elements used in process control industry [1]. In practice, operational amplifiers are generally used in analog controllers. On the other hand, current-mode (CM) circuits such as second-generation current conveyors (CCII) and current feedback amplifiers (CFOA) have considerable attention due to their wider frequency band, lower power consumption, better linearity and stability properties compared to their voltage-mode counterparts, operational amplifiers [2-5]. These CM circuits have not been used in design of analog controllers except the one by Erdal *et. al*. [6] so far. The purpose of this study is to present a new PID circuit. In this circuit, CCIIs are used as current followers in such a way that voltage tracking non-idealities are excluded. The signal-flow graph approach is used to facilitate the design. The circuit presented in this work employs also a minimum number of CCIIs for the general transfer function realization of a PID controller. To verify the theory, the simulation of the proposed circuit is performed and the results are discussed. Then, the optimum parameter tolerances are determined by the use of parameter sensitivities. These tolerances keep the relative error of the output voltage of the controller in tolerance region and they can also be used to improve and to control the sensitivity performance of the proposed PID controller.

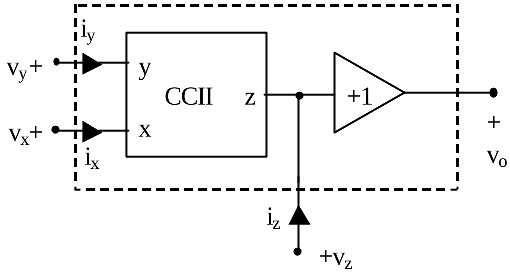
2. CURRENT CONVEYOR

The terminal relationships of the positive and negative type CCIIs (CCII+ and CCII-) shown in Fig 1. are given as follows [7]:

$$i_y(t) = 0\,,\;\; v_x(t) = v_y(t)\,,\;\; i_z(t) = \pm\, i_x(t) \qquad (1)$$



(a)



(b)

Figure 1.(a) Circuit symbol of second-generation current conveyor (CCII)
(b) Circuit symbol of current feedback amplifier (CFOA)

Attaching a unity gain voltage buffer at the output of the CCII, which is actually a a current feedback operational amplifier, CFOA, enables easy cascading in voltage-mode operation because of the low output impedance of the buffer. Thus, the proposed PID controller can also be realized by using of CFOAs.

Taking the non-idealities of the CCII into account Eq. (1) can be rewritten as follows:

$$i_y(t) = 0\,,\;\; v_x(t) = \beta\, v_y(t)\,,\;\; i_z(t) = \pm\,\alpha\, i_x(t) \quad (2)$$

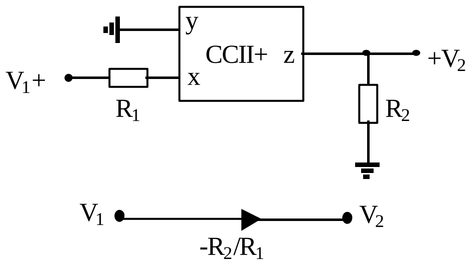
Here $\alpha = 1-\varepsilon_i$ denotes the current gain and $\beta = 1-\varepsilon_v$ denotes the voltage gain of the current conveyor, ε_i, ($|\varepsilon_i|$<<1) is the current tracking error and ε_v, ($|\varepsilon_v|$<<1) is the voltage tracking error. The non-ideal effect of the voltage buffer can similarly be given as follows:

$$v_o = \gamma v_i\,,\quad \gamma = 1-\varepsilon_o\,,\quad |\varepsilon_o| << 1 \qquad (3)$$

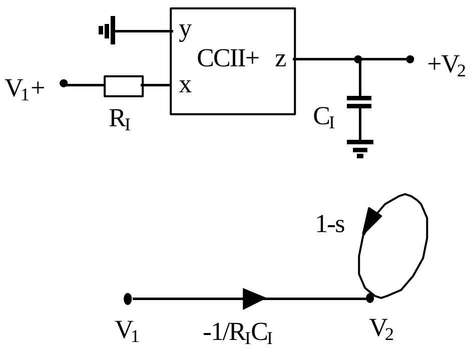
Here γ is the voltage gain, v_o is the output voltage of buffer, and ε_o is the voltage tracking error of the voltage buffer.

3. SYNTHESÝS PROCEDURE

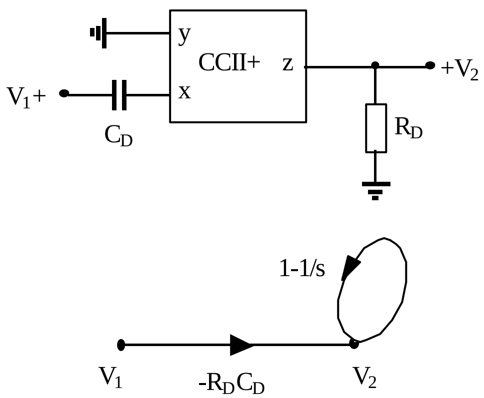
Consider the current conveyor circuits shown in Fig. 2. The signal-flow graphs of these circuits can be drawn by using the defining equations of CCII [8,9].



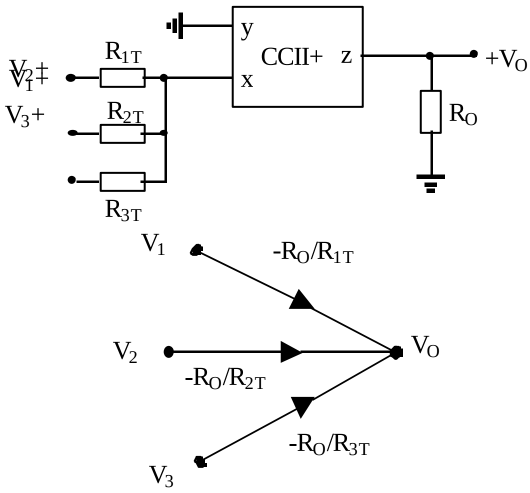
(a) Amplifier circuit



(b) Integrator circuit



(c) Derivative circuit



(d) Summing circuit

Figure 2. Basic building blocks using CCIIs together with corresponding signal-flow graphs

In Fig. 2(a), an amplifier circuit and its signal-flow graph are shown. The gain is $-R_2/R_1$ as it can be easily seen from its signal-flow graph. In Fig. 2(b), an integrator and its signal-flow graph are shown. The integration time constant of this circuit is $-1/R_IC_I$. In Fig. 1(c), a CCII based derivative circuit and corresponding signal-flow graph are illustrated. The derivation time constant of this circuit is $-R_DC_D$. To obtain PID controller the three basic operations shown in Figs. 2 (a), (b), and (c) are transmitted to the output by CCII based summing circuit shown in Fig. 2(d). Note that, all the sub-circuits illustrated in Fig.2 are inverting circuits. If a given transfer function is represented by a signal flow-graph, it can be easily observed from Fig. 2 that the corresponding circuit to the given transfer function can be realized by interconnecting these building blocks [10,11]. Note also that, in non-ideal case all the transfer functions shown in Fig. 2 should be multiplied by the factor of α. If voltage buffers are used this factor modifies to $\alpha\gamma$.

The transfer function of a general analog, proportional-integral-derivative controller can be written as follows:

$$T(s) = K_P + \frac{K_I}{s} + sK_D \qquad (4)$$

A signal-flow graph of the transfer function of an analog PID controller can be drawn such as in Fig. 3 [9].

The realization of the analog CCII based PID controller circuit corresponding to the signal-flow graph in Fig. 3, which is realized by the sub-circuits in Fig. 2, and unity gain voltage buffers is shown in Fig.4.

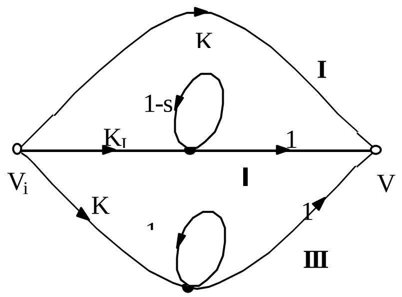


Figure 3. Signal flow graph corresponding to the transfer function of the general proportional-integral-derivative (PID) controller

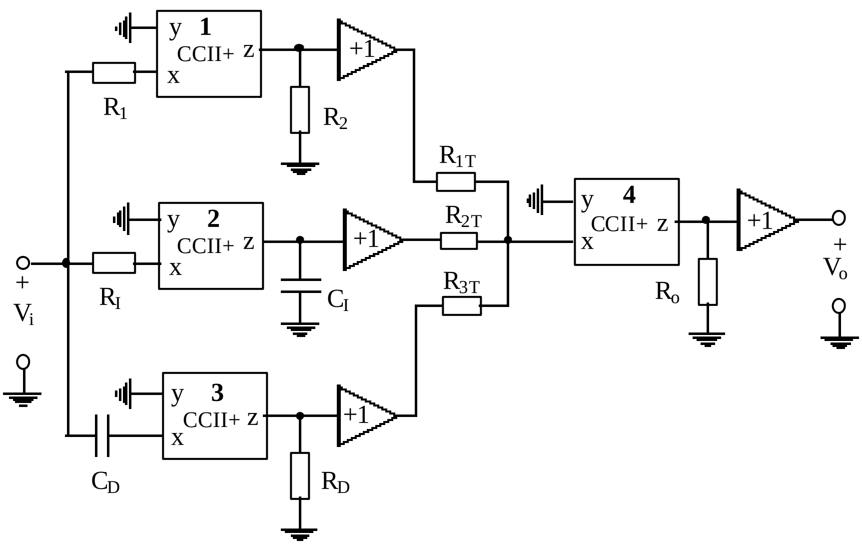


Figure 4. CCII based PID controller realization corresponding to the signal-flow graph in Fig. 3

In Fig. 4, a CCII based PI controller circuit and a CCII based PD controller circuit can also be obtained by removing path III and path II, respectively.

If the circuit in Fig. 4 is analyzed the controller coefficients K_P, K_I, and K_D will be obtained as follows:

$$K_P = \alpha_1\gamma_1\alpha_4\gamma_4 \frac{R_2 R_O}{R_1 R_{1T}}, \qquad (5a)$$

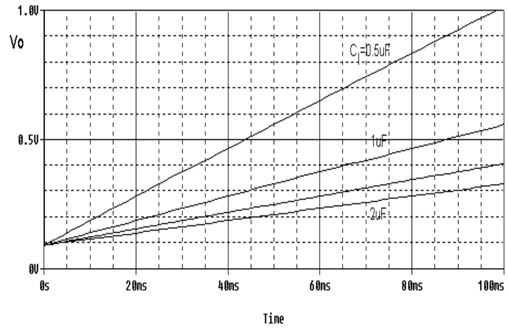
$$K_I = \alpha_2\gamma_2\alpha_4\gamma_4 \frac{R_O}{R_I C_I R_{2T}}, \qquad (5b)$$

$$K_D = \alpha_3\gamma_3\alpha_4\gamma_4 \frac{R_D C_D R_O}{R_{3T}}. \qquad (5c)$$

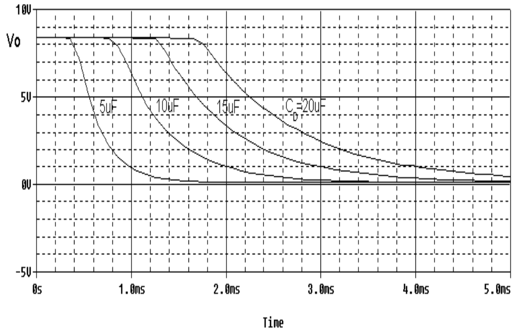
4. THE RESULTS OF SIMULATION

In order to confirm the theoretical results, the PID circuit given in Fig. 4 is simulated in the SPICE program by using the macro-model of AD844/AD from Analog Devices. In this circuit, supply voltages of ± 12V and in order to illutrate the time-domain response, the step input voltage with 1 Volt amplitude are used. In simulation procedure, the values of the capacitors C_I and C_D, the resistor values, and the input voltages also are given in the caption of Fig. 5. The capacitance values are selected such as to have a better illustration.

The simulation results of the output of the CCII based PID controller are given in Figure 5 (a) and (b) respectively. In both situations, the proportional gains are taken to be zero in order not to confuse the figures.



(a)



(b)

Figure 5. Results of the simulation of the PID controller in Fig. 4

(a) Output waveform of the PID controller for step response of the input with 1V amplitude and R_I=50kΩ, R_D=50kΩ, C_D=0.1μF and C_I as parameter from 0.5μF to 2μF (R_O=10kΩ, R_1=2kΩ, R_2=10kΩ, R_{1T}=5MΩ, R_{2T}=40kΩ,R_{3T}=1kΩ)

(b) Output waveform of the PID controller for step response of the input with 5mV amplitude and R_I=50kΩ, R_D=50kΩ, C_I=1μF and C_D as parameter from 5μF to 20μF (R_O=10kΩ, R_1=2kΩ, R_2=10kΩ, R_{1T}=5MΩ, R_{2T}=40kΩ, R_{3T}=1kΩ)

From Figs. 5 (a) and (b), it is clear that the results are in good agreement with the theoretical expectations.

5. CALCULATING OPTIMUM PARAMETER TOLERANCES

The optimum parameter tolerances are defined as the tolerances contribute equally to the upper bound of the relative error of the output voltage of the controller ($|\Delta V_o/V_o|$) given in Fig. 4. In general, it is not known in advance how much each parameter contributes to the output error. That is why this definition is quite reasonable, since the designer expects the contribution of each parameter variation on output deviation to be equal to each other. The formulation of these tolerances was given by Erdal *et. al.* [9].As a result, we can define the optimum parameter tolerances as

$$t_{x_i} = t_0 / n\left|S_{x_i}^{T}(\omega_i)\right|_{max}, \quad i = 1,\ldots,18 \qquad (6)$$

where t_{x_i} is the ith parameter tolerance, t_0 is the output tolerance of the controller, n is the parameter number, i.e. n=18 for the given configuration, and ω_i is the angular frequency at which $\left|S_{x_i}^{T}(\omega)\right|$ takes its maximum value, i.e.

$$\left|S_{x_i}^{T}(\omega_i)\right|_{max} = \max\left\{\left|S_{x_i}^{T}(\omega)\right|\right\}, \quad \omega\in[\omega_1,\omega_2] \qquad (7)$$

where $\omega\in[\omega_1,\omega_2]$ describes designer's specified frequency band. Hence $\left|S_{x_i}^{T}(\omega)\right| \le \left|S_{x_i}^{T}(\omega_i)\right|_{max}$, $\omega\in[\omega_1,\omega_2]$. It should be noted that ω_i belong to the interval $\omega\in[\omega_1,\omega_2]$, and $\left|S_{x_i}^{T}(\omega)\right|$ has its maximum value at this frequency. The designer can easily determine ω_i by plotting $\left|S_{x_i}^{T}(\omega)\right|$ at this interval or by using already existing mathematical programs like Matlab.

For example, assuming that the proportional gain, K_P =10, the integral gain, K_I =2 s^{-1}, and the derivative gain, K_D =5 s, are given. Then the parameter values can be selected in Fig. 4 as follows:

$$R_o = 10K\Omega,\ R_1 = 2K\Omega,\ R_2 = 20K\Omega, \qquad (8a)$$
$$R_I = 50K\Omega,\ R_D = 50K\Omega, \qquad (8b)$$
$$R_{1T} = 5K\Omega,\ R_{2T} = 40K\Omega,\ R_{3T} = 1K\Omega, \qquad (8c)$$
$$C_I = 1\,\mu F,\ C_D = 10\,\mu F, \qquad (8d)$$
$$\alpha_i = 1,\ i = 1...4,\ \gamma_k = 1,\ k = 1...4. \qquad (8e)$$

For this example, the maximum values of the parameter sensitivities are calculated as follows:

$$\left|S_{x_i}^{T}(\omega_i)\right|_{max} = 1, \quad i = 1,\ldots,18 \qquad (9)$$

If it is required that $|\Delta V_o/V_o| \le 0.1$ the parameter tolerances are to be chosen as follows:

$$t_{R_1} = t_{R_2} = t_{R_o} = t_{C_I} = t_{C_D} = 0.55\% \, , \qquad (10a)$$

$$t_{R_{1T}} = t_{R_{2T}} = t_{R_{3T}} = 0.55\%, \qquad (10b)$$

$$t_{\alpha_i} = t_{\gamma_i} = 0.55\% \, , \quad i = 1,\ldots,4 \, . \qquad (10c)$$

For this particular example, the optimum tolerances are found to be equal to each other, however they are usually different in general case. Choosing the parameter tolerances such as above, the designer can guarantee that the maximum deviation of the output voltage of the controller caused by the parameter variations due to the environmental effects will be less than or equal to 0.1. This result can also be verified in SPICE simulation. If $|\Delta V_o/V_o| \leq 0.01$ is required the parameter tolerances must be chosen ten times smaller than the ones in Eq. (10) and so forth.

6. CONCLUSIONS

In this study, a CCII based PID design procedure is given and a new PID circuit is proposed. This circuit consists of only four CCIIs, two grounded capacitors, eight resistors, and four voltage buffers and it is very convenient for integrated circuit implementation. It is also very suitable stable and fast control due to the enhanced properties of the current-mode circuits used in the design. Considering that, the controller coefficients K_P, K_I, and K_D are depended on the time constants and resistor ratios they can easily be adjusted to any desired value independently from each other. Furthermore, the optimum parameter tolerances are determined to keep the relative error of the output of the CCIIs based PID controller due to parameter variations in its tolerance region.

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